

ABSTRACT OF THE DISCLOSURE

A method and apparatus for 2x oversampling of data having jitter. In some  
embodiments, the invention is a clock and data recovery device including an alternating  
5 edge sampling binary phase detector, and which is configured to stabilize loop  
characteristics in various jitter environments and can be implemented with small  
hardware overhead. A transceiver that embodies the invention can be implemented as a  
CMOS integrated circuit using a 0.18 $\mu$ m CMOS process, with the transceiver chip  
being capable of recovering data having a data rate of up to 11.5 Gbps from a signal  
10 received over a serial link, while consuming no more than 540mW from 1.8V supply,  
and with a bit error rate of less than  $10^{-12}$ .